

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:)
CAPPELLETTI)
)
Serial No. **Not Yet Assigned**)
)
Filing Date: **Herewith**)
)
For: **METHOD OF MAKING FLOATING GATE**)
NON-VOLATILE MEMORY CELL WITH)
LOW ERASING VOLTAGE)
HAVING DOUBLE LAYER GATE)
DIELECTRIC)
)

This application is a divisional of Serial No. 10/158,706 filed May 30, 2002, which is a divisional of Serial No. 09/521,876 filed March 8, 2000, now U.S. Patent No. 6,399,444, which is a divisional of Serial No. 08/940,856 filed September 29, 1997, now U.S. Patent No. 6,054,731

PRELIMINARY AMENDMENT

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Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

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NAME: Justin Goree

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In re Patent Application of:

CAPPELLETTI

Serial No. **Not Yet Assigned**

Filing Date: **Herewith**

In the Title:

Please delete the current title and substitute:

**-- METHOD OF MAKING FLOATING GATE NON-VOLATILE MEMORY
CELL WITH LOW ERASING VOLTAGE HAVING DOUBLE LAYER GATE
DIELECTRIC --**